REMARKS

This paper is responsive to the Non-Final Office Action dated September 2, 2004. Claims 1-27 and 31-33 were examined. Claims 1-13, 21-27, and 31-33 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Baweja (U.S. Pat. No. 6,212, 599). Applicant appreciates the indication that claims 14-20 are allowed. By way of the present amendment claim 8 is being canceled.

Claim 1 has been amended to recite supplying the memory control signal from another location in the computer system, the other location in the computer system being independent of the first integrated circuit during normal operation, when the computer system is in a power savings state to maintain memory in the self refresh state. In contrast Baweja teaches at col. 4, lines 33-34, that during normal operation suspend memory controller 210 acts as part of the memory system controller 200. Accordingly, applicant respectfully submits that suspend memory controller 210 is not independent of memory system controller 200 and that claim 1 and all claims dependent thereon distinguish over Baweja and the other references of record.

Applicant respectfully disagrees with the Office Action that it is well known and common practice in the art to use an AND gate or tristate buffer as an isolating circuit to allow the same signal to be controlled by two different locations. An AND gate provides a logical function while the circuit taught in Fig. 5 of the application functions to electrically isolate circuits. Further, a tristate buffer allows another output buffer to drive a signal line to a 1 or 0 while the tristate buffer is generating a high impedance signal. An AND gate can perform no such function. Instead the AND gate has to be coupled to both locations in order to work correctly. Thus, such functions are clearly not the same. In accordance with MPEP § 2144.03 applicant respectfully traverses the Examiner's Official Notice and requests the Examiner provide a reference showing that this is well known and common practice to use an AND gate or tristate buffer as stated in the Office Action. Applicant notes that while "isolation" is not recited in claim 1, isolation and high impedance (from a tristate buffer) is relevant in other claims.

Claim 9 has been put in independent form and recites that the isolating further includes disabling a switch coupling the memory control signal from the first integrated circuit to the memory by driving a switch enable signal to a first predetermined value to turn off the switch,

the switch enable signal being driven from the other location. With respect to claim 9, applicant respectfully disagrees with the Examiner's position that a switch capable of outputting high-impedance level is inherent in Baweja in order to isolate the clock enable signals between the two memory controller (210 and 220). In fact, Fig. 3 shows an AND gate is used to logically combine SDSCKE 240 and SCKE generated by suspend well 220. Thus, a switch is not inherent or needed in Baweja. Further, applicant submits that Baweja fails to teach a switch enable signal being driven from suspend well 220. Accordingly, applicant submits that claim 9 and all claims dependent thereon distinguish over the references of record.

Claim 21 has been amended to recite that the output terminal is coupled to supply a control value at the first logic level to maintain the system memory in a self refresh state when the first means is completely powered off. Claim 21 additionally recites first means for controlling system memory during an operational state; and second means, for controlling the system memory during a power savings state to maintain the system memory in a self refresh state when the first means is completely powered off, the second means including means for holding an output terminal at a high impedance during the operational state and means for providing a first logic level through the output terminal during the power savings state.

With regards to claim 21 applicant respectfully submits that Baweja fails to teach holding an output terminal at high impedance during an operational state and providing a first logic level through the output terminal during the power savings state to maintain the system memory in a self refresh state when the first means is completely powered off. Corresponding structure to claim 21 is shown in, e.g. Figs. 2 and 5, where signal line 218 is supplied as the CKE signal in a power savings state and is held at high impedance during operational states. The Office Action points to col. 5, lines 16-21 in discussing claim 10, stating the signal line is driven at a high impedance by the second memory controller 220 during the operational state. In fact, that portion of Baweja states:

> *Because the CKE signal is the output of an AND logic 320, if either SCKE or SDKE signal is the low, the CKE signal is low. Therefore, the status of the SDCKE signal 240 is irrelevant if the SCKE signal 315 is maintained low.*

There is simply no teaching of a high impedance signal. In fact, there is no teaching of suspend well 220 ever generating a high impedance signal. Instead, Baweja simply recites the function of an AND gate that if one of the inputs is low, the other input is a "don't care." Accordingly, applicant respectfully submits that Baweja fails to teach the recited function or corresponding structure of claim 21 and therefore claim 21 and all claims dependent thereon distinguish over Baweja.

With regards to claim 24, applicant respectfully submits that Baweja fails to teach or suggest a first output terminal for coupling to a memory control signal that is held at a first logic level to keep a memory in a self refresh state, the integrated circuit responsive to a first operational state of the computer system to place the output terminal at a high impedance level and responsive to a power savings state in the computer system to supply the first logic level on the output terminal. Figs. 2 and 5 shows an exemplary structure, where signal line 218 is supplied as the CKE signal in a power savings state and is held at high impedance during operational states. In contrast, Baweja utilizes and AND gate 320 (see Fig. 3 of Baweja) to combine the control signals from suspend well 220 and the first memory controller 210. There is no teaching or suggestion to modify Fig. 2 or 3 of Baweja to achieve the output terminal generating a high impedance level during a first operational state as recited in claim 24. Accordingly, applicant respectfully submits that claim 24 and dependent claim 25 distinguish over the art of record.

With respect to claim 26, applicant respectfully submits that Baweja fails to teach an asserted reset signal holds the memory control signal at the first value (self refresh state) during the power savings state. The Office Action points to col. 6, lines 22 et. seq. (in discussing claim 5). Applicant points out that Baweja teaches in Fig. 4, that the reset signals PCIRST# and CPURST# are not even asserted while main power is off. Thus, those resets can not be used as claimed to hold the memory control signal at the first value (self refresh state) during the power savings state. Instead, Baweja teaches that the resets are used to reset the registers. Col. 6, lines 34-35. Thus, applicant respectfully submits that claim 26 and all claims dependent thereon distinguish over Baweja and the other references of record.

With respect to claim 31, applicant respectfully submits that Baweja fails to teach , a reset signal that, when asserted, causes the second circuit to keep the memory control signal at the logic level to maintain the memory in a self refresh state. The Office Action points to col. 6, lines 22 et. seq. (in discussing claim 5). Applicant points out that Baweja teaches in Fig. 4, that the reset signals PCIRST# and CPURST# are not even asserted while main power is off. Thus, those resets can not be used during the power savings state to keep the memory control signal at the logic level to maintain the memory in the self refresh state. Instead, Baweja teaches that the resets are used to reset the registers. Col. 6, lines 34-35. Thus, applicant respectfully submits that claim 31 and all claims dependent thereon distinguish over Baweja and the other references of record.

In summary, claims 1-7, 9-27 and 31-33 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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Mark Zagorin 11/30/04
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Respectfully submitted,

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